IBM INDUSTRIAL PRODUCTS

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ISOLATING INVERTER (II-1A) MODULE P/N 841579

361479

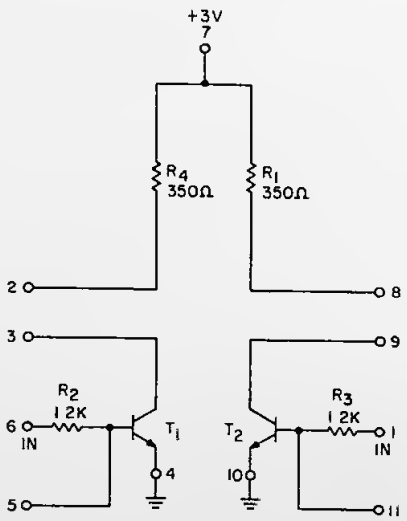
Functional Description

The Isoloting Inverter, II-1A module contoins two isoloting inverters. The resistor coupled input will load down the narmol up level of the driving block, however, the minimum up level is still obave the threshold levels af the AI-2A, AOI-1A ond AOI-2A modules. The driving module can hove both II-1A ond diode logic circuits as laods.

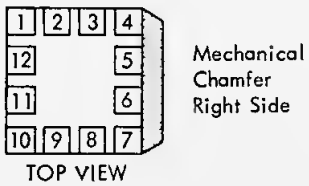
The "OR" function con be accomplished by dotting collectors (parollel connected collectors) with other circuits or modules. However, only one collector resistor is required.

The driving source must hove an equivolent resistonce af 375 ar lower ta +3V when driving two II-1A's.

Schematic

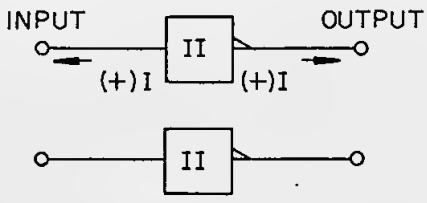


Terminal Configuration



Pins 5, 11 and 12 Leave Open

Block Diagram



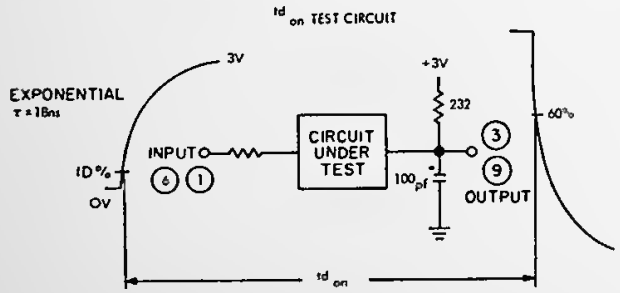
Maximum Ratings

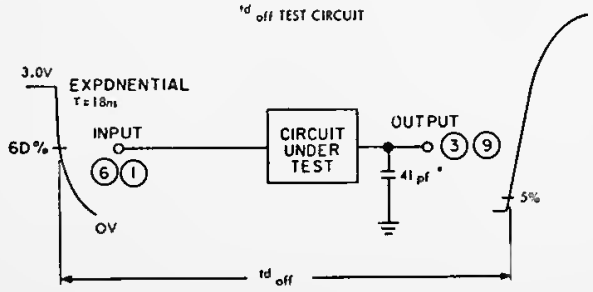
Input Voltage = 6V
Output Voltage = 6V
I_E = 30 Milliamps

II-1A Module Functional Tests

TESTS	TERMINAL CONDITIONS												°C	ADDITIONAL LOAD REQUIREMENTS	VARIABLE	LIMITS		UNITS
	1	2	3	4	5	6	7	8	9	10	11	12				MIN	MAX	
DC ON		V_0	V_0	GND		+2V	+3.12V						25/75	18.3ma CURRENT INTO TERMINAL 3	V_0		0.3/0.31	V
DC ON	+2V						+3.12V	V_0	V_0	GND			25/75	18.3ma CURRENT INTO TERMINAL 9	V_0		0.3/0.31	V
DC NOISE		V_0	V_0	GND	+0.58V		+2.88V						75		V_0	1.8		V
DC NOISE							+2.88V	V_0	V_0	GND	+0.58V		75		V_0	1.8		V
td_{on}		100 pf CAP TO GND	V_0	GND		INPUT	+3V						25	232Ω RESISTOR TIED BETWEEN TERM. 2&7	td_{on}	14	36	ns
td_{on}	INPUT						+3V	100 pf CAP TO GND	V_0	GND			25	232Ω RESISTOR TIED BETWEEN TERM. 7&8	td_{on}	14	36	ns
td_{off}		41 pf CAP TO GND	V_0	GND		INPUT	+3V						25/75		td_{off}	14	41/56	ns
td_{off}	INPUT						+3V	41 pf CAP TO GND	V_0	GND			25/75		td_{off}	14	41/56	ns
DC OFF		TO PIN 3	V_{OUT}	GND	+0.5V		2.88V						25		V_{OUT}	2.84		V
DC OFF							2.88V	TO PIN 9	V_{OUT}	GND	+0.5V		25		V_{OUT}	2.84		V

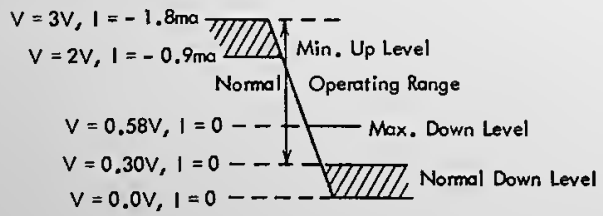
Test Waveforms



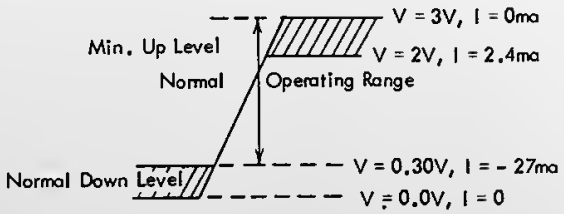


* Including Probe Capacitance

Input Requirements



Output Specifications



Fan Out

Total available collector current = 27ma

$27ma \geq I_R + N_1 K_1 + N_2 K_2 + - - -$

I_R = Current through collector resistor

N_1 = Number of AI-2A loads being driven

N_2 = Number of AOI-2A loads being driven

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K_1 = AI - 2A loading constant = 2.3mo

K_2 = AOI -2A loading constant = 3.0ma

To double the Fan Out, the output collectors and inputs must be paralleled.

Maximum Power Supply Current Requirements (per circuit)

	ON	OFF
+6V	0	0
+3V	8.8mo	0
-3V	0	0

Maximum Power Dissipation (per circuit)

ON	OFF
17.65	0

Average Normal Power Dissipation $= \frac{\text{NOMINAL ON + NOMINAL OFF}}{2} = 15\text{mw/circuit}$

General Wiring Rules (For Printed Circuit Wire - 10 Mil Width Lines)

The input single line length should be less than 12 inches to prevent excessive noise coupling. The total net length of either input or output should be less than 60 inches unless longer delays can be tolerated.